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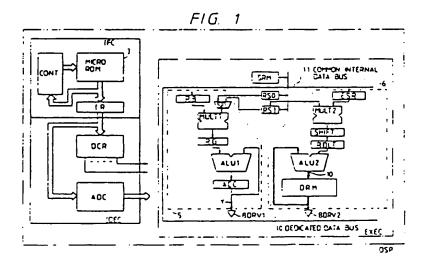
Date of deferred publication of the search report: 09.03.94 Bulletin 94/10 Applicant: HITACHI, LTD.
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- Arithmetic circuit, and adaptive filter and echo canceler using it.
- n the digital signal processor used for realizing application filters, the filter output calculation processing system 5 and the tap coefficient update calculation processing system 6 are separated. In the update calculation processing system 6, the integrating calculation for the tap coefficient updating that requires read and write operations on the data memory DRM is performed in one machine cycle by

using the dedicated data bus 10 and executing the read-modify-write operation on the data memory. As a result, to the extent that the time taken by the integrating processing which has conventionally required two machine cycles can be shortened, the operation clock frequency can be lowered to reduce the power consumption while maintaining the processing capability per unit of time.



EUROPEAN SEARCH REPORT

Application Number EP 92 10 4526

ucgory	Citation of document with int of relevant pass		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.CL5)	
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EUROPEAN SEARCH REPORT

Application Number EP 92 10 4526

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